

MOSIN MONDAL

Member of Consulting Staff
Cadence Design Systems (I) Pvt. Ltd.

<http://www.mosinmondal.com>

Plot Nos. 57A B & C
NOIDA Special Economic Zone
P.O. – NSEZ, NOIDA, U.P. 201305 INDIA
Phone: +91 120 3984000 Ext. 4014

AREAS OF INTEREST

On-chip and off-chip power and signal integrity, circuit-electromagnetic co-simulation, computational geometry, DRC checking, interconnect modeling, CAD for VLSI systems.

EDUCATION

PhD in Electrical Engineering

University of Washington, Seattle, USA (March 2007 - December 2009)

Dissertation Title: Computational Techniques for Power and Signal Integrity in Packaged Microelectronics

Advisor: Prof. Vikram Jandhyala

MS in Electrical and Computer Engineering

Rice University, Houston, USA (August 2004 – February 2007)

GPA: 4.0/4.0

BE (Honors) in Electronics and Telecommunication Engineering

Jadavpur University, Calcutta, India (July 1997 – June 2001)

GPA: 3.83/4.0

INDUSTRIAL EXPERIENCE

Cadence Design Systems (I) Pvt. Ltd., NOIDA, India, as **Member of Consulting Staff** (January 2010 – present)

– In the development group of **Virtuoso Space Based Router and Design Rule Checker**

IBM Corporation, RTP, USA as **Technical Co-op** (June – December, 2007) in the tools development group:

– **PowerPEEC** (IBM's full wave circuit-EM simulation tool)

- Enhanced the efficiency, robustness and stability of the core engine of the tool
- Significantly reduced the computation time for partial inductance and capacitance
- Modeled and simulated different board and package components using PowerPEEC

– **Crosstalk aware rule checking in board level**

- Efficient crosstalk aware rule checking
- Developed method for fast estimation of parasitic elements for striplines and microstrips
- Implemented fast crosstalk estimation algorithm

– **Analysis of non-ideal common ground connection in multi-board PCBs**

- Analysis of SI and EMI issues due to non-ideal “common ground” in multi-board PCBs
- Efficient inductance estimation for connector pins that cause impedance discontinuity
- Optimal pin-assignment to reduce electromagnetic interference

Cadence Design Systems (I) Pvt. Ltd., NOIDA, India, as **Software Engineer** (July 2001 – March 2003) and

Member of Technical Staff (April 2003 – May 2004) in the development team of:

– **CeltIC** [Currently part of Encounter Timing System (ETS)] (Crosstalk glitch and delay analyzer, 2002-2004)

- Worked on cell characterization techniques
- Worked on noise and delay computation modules
- Developed techniques for incorporating on-chip variation (OCV) effects
- Gained overall knowledge of the entire flow and experience using Berkeley SPICE engine

– **PCB Librarian Expert** (Cell library creation and management tool for PCB, 2001)

- Designed and implemented basic data structures around Microsoft Foundation Classes (MFC)
- Designed and implemented different parser modules
- Designed and implemented generic, configurable graphical interfaces
- Developed different import/export modules for interlibrary and inter-tool cell exchange

GRADUATE RESEARCH EXPERIENCE

- **Power integrity (PI) modeling and simulation in package and board levels (2008-2009)**
 - Modeling of power delivery networks for power integrity analysis
 - Development of a full-fledged simulation tool in C++ for PI analysis
 - Efficient finite difference scheme for analyzing real-life boards and packages
 - Macromodeling technique for decoupling capacitor optimization
- **Ray tracing for radio frequency identification (RFID) systems (2009)**
 - Estimation of field and power at any location in a given site
 - Development of a ray tracing tool in C++
- **Analytical modeling of on-chip inductance (2004-2005)**
 - Development of an analytical model for on-chip frequency dependent loop self-inductance
 - Modeling based on generalizing the response of simple loops to more complicated loops
 - Can be applied for accurate RLC wire delay estimation of a wide range of wire geometries
- **Design of thermally robust clock tree (2006-2007)**
 - Analysis of temperature gradient vs. clock skew using BSIM3 device model and PEEC interconnect model
 - Proposed dynamically adaptive technique for minimizing temperature-dependent skew
 - Designed clock buffers that dynamically adjust the driving strength with surrounding temperature
 - Extended the technique for application in 3-D integrated circuits
- **Analysis of gate-level noise robustness under parameter variations (2006-2007)**
 - Analysis of noise immunity of digital gates under parameter variations
 - Analytical approach developed for estimating the noise susceptibility of gates
 - Orders of magnitude performance gain over circuit simulations
- **Analysis of delay variation in network-on-chip (NoC) interconnects due to process variations (2006)**
 - Development of Elmore delay-based analytical technique for delay variability in buffered NoC link
 - Estimation of link failure probability due to delay variation
- **Analysis of crosstalk induced dynamic power (2006)**
 - Developed method for estimating the additional switching and short circuit energy
 - Proposed a heuristic for computing the extra energy spent by a switching victim net

COMPUTER SKILLS

- **Programming Languages:** C++, C. Proficient in object oriented programming.
- **Scripting Languages:** PERL, TCL
- **Mathematical Tools:** MATLAB, Mathematica
- **Circuit and EM Simulation Tools:** SPICE, PowerPEEC, PhysWAVE, Ansoft HFSS
- **IC Design Platform:** Cadence Virtuoso
- **Operating Systems/Environments:** UNIX, Windows

AWARDS AND HONORS

- IEEE EMC Society President's Memorial Award, 2008-2009
- Best Paper Award at the IEEE Electrical Performance of Electronic Packaging (EPEP) Conference, 2007
- Research Assistantship, Dept. of EE, University of Washington, 2007 - 2009
- Rice University Graduate Fellowship, Research Assistantship, 2004-2006
- Excellence in Execution Award, Cadence Design Systems, 2004
- 2nd in Bachelor of Engineering in Electronics, Jadavpur University, 2001
- Governor's Gold Medal for all-round academic performance, 1997
- 3rd (out of 300,000) in the state of West Bengal in Higher Secondary (10+2) Examination, 1997
- 4th (out of 50,000) in the West Bengal Joint Entrance Examination, 1997
- 11th (out of 400,000) in the state of West Bengal in Secondary (10th) Examination, 1995
- National Talent Scholarship from National Council for Education, Research and Training (NCERT), 1995

PUBLICATIONS

1. **Mosin Mondal**, James Pingenot and Vikram Jandhyala, "Efficient Hierarchical Discretization of Off-chip Power Delivery Network Geometries for 2.5D Electrical Analysis," in *Proceedings of the International Symposium on Quality Electronic Design (ISQED)*, March 2010.
2. **Mosin Mondal**, Bruce Archambeault and Vikram Jandhyala, "Enabling Early Design of Complex Power Delivery Networks Using Spatially-Nonuniform Finite-Difference Method," DesignCon, February 2010.
3. Tamer Ragheb, Andrew Ricketts, **Mosin Mondal**, Sami Kirolos, Greg Link, Vijaykrishnan Narayanan and Yehia Massoud, "Design of Thermally Robust Clock Trees Using Dynamically Adaptive Clock Buffers," *IEEE Transactions on Circuits and Systems - I*, vol. 56, no. 2, pp. 374-383, February 2009.
4. **Mosin Mondal**, Samuel Connor, Bruce Archambeault and Vikram Jandhyala, "Including the Impact of Connecting Vias in the Performance Metric Evaluation for Board-Level Optimization of Decoupling Capacitors", in *Proceedings of IEEE Electrical Performance of Electrical Packaging (EPEP)*, October 2008.
5. **Mosin Mondal**, Samuel Connor, Bruce Archambeault and Vikram Jandhyala, "Fast Frequency Domain Crosstalk Analysis for Board-Level EMC Rule Checking and Optimization," in *Proceedings of IEEE EMC Symposium*, August 2008.
6. Samuel Connor, Bruce Archambeault and **Mosin Mondal**, "The Impact of Common Mode Currents on Signal Integrity and EMI in High-Speed Differential Data Links," in *Proceedings of IEEE EMC Symposium*, August 2008.
7. Samuel Connor, Bhyrav Mutnury, **Mosin Mondal**, Pravin Patel, Jay Diepenbrock, Moises Cases and Bruce Archambeault, "The Impact of Common Mode Currents and Interconnect Inductance on the Signal Quality of Differential Signals in Multi-Board PCB Systems," in *Proceedings of DesignCon*, February 2008. (**Best Paper Nomination**)
8. **Mosin Mondal** and Yehia Massoud, "Accurate Analytical Modeling of Frequency Dependent Loop Self-inductance," *Journal of Circuits, Systems, and Computers*, vol 17, no. 1, pp. 77-93, February 2008.
9. **Mosin Mondal**, Bhyrav Mutnury, Pravin Patel, Samuel Connor, Bruce Archambeault and Moises Cases, "Electrical Analysis of Multi-board PCB Systems with Differential Signaling Considering Non-ideal Common Ground Connection," in *Proceedings of IEEE Electrical Performance of Electrical Packaging (EPEP)*, October 2007. (**Best Paper Award**)
10. Sami Kirolos, **Mosin Mondal**, Kartik Mohanram and Yehia Massoud, "A Model-Based Technique for Efficient Evaluation of Noise Robustness," in *Proceedings of the IEEE International Symposium on Circuits and Systems (MWSCAS)*, August 2007.
11. **Mosin Mondal** and Yehia Massoud, "A Methodology for the Estimation of Capacitive Crosstalk-Induced Short-Circuit Energy," *Journal of Circuits, Systems, and Computers*, vol. 16, no. 3, pp. 455-465, June 2007.
12. **Mosin Mondal**, Sami Kirolos and Yehia Massoud, "Estimation of Capacitive Crosstalk-Induced Short-Circuit Energy," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, May, 2007.
13. **Mosin Mondal**, Andrew Ricketts, Sami Kirolos, Tamer Ragheb, Greg Link, Vijaykrishnan Narayanan and Yehia Massoud, "Thermally Robust Clocking Schemes for 3D Integrated Circuits," in *Proceedings of Design Automation and Test in Europe (DATE)*, April 2007.
14. **Mosin Mondal**, Andrew Ricketts, Sami Kirolos, Tamer Ragheb, Greg Link, Vijaykrishnan Narayanan and Yehia Massoud, "Mitigating Thermal Effects on Clock Skew with Dynamically Adaptive Drivers," in *Proceedings of the International Symposium on Quality Electronic Design (ISQED)*, March 2007.
15. **Mosin Mondal**, Kartik Mohanram and Yehia Massoud, "Parameter-Variation-Aware Analysis for Noise Robustness," in *Proceedings of the International Symposium on Quality Electronic Design (ISQED)*, March 2007.
16. **Mosin Mondal**, Xiang Wu, Tamer Ragheb, Adnan Aziz and Yehia Massoud, "Provisioning On-Chip Networks under Buffered RC Interconnect Delay Variations," in *Proceedings of the International Symposium on Quality Electronic Design (ISQED)*, March 2007.
17. Arthur Nieuwoudt, **Mosin Mondal** and Yehia Massoud, "Predicting the Performance and Reliability of Carbon Nanotube Bundles for On-Chip Interconnect," in *Proceedings of the Asia and South Pacific Design Automation Conference (ASPDAC)*, January 2007.

18. **Mosin Mondal** and Yehia Massoud, "Accurate Loop Self Inductance Bound for Efficient Inductance Screening," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 12, pp. 1393-1397, December 2006.
19. **Mosin Mondal**, Xiang Wu, Adnan Aziz and Yehia Massoud, "Reliability Analysis for On-chip Networks under RC Interconnect Delay Variation", in *Proceedings of the International Conference on Nano-Networks*, Lausanne, Switzerland, September 2006.
20. **Mosin Mondal** and Yehia Massoud, "Reducing Pessimism in RLC Delay Estimation Using an Accurate Analytical Frequency Dependent Model for Inductance", in *Proceedings of IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, pp. 691-696, November 2005.
21. **Mosin Mondal** and Yehia Massoud, "Analytical Modeling of Loop Self Inductance Bound for Inductance-Aware Physical Synthesis", in *Proceedings of IEEE International Symposium on Circuits and Systems (MWSCAS)*, August 2005.

CONTRIBUTED BOOK CHAPTER

"Power Integrity Analysis and EMI/EMC" in *Power Integrity Analysis and Management for Integrated Circuits*, published by Prentice-Hall, May, 2010.

RELEVANT GRADUATE LEVEL COURSES

Electromagnetic Computations and Applications	VLSI Design: Theory & Application
Microwave Engineering	Low Power VLSI Design
High Speed Integrated Circuits	VLSI Design: Datapath and Memory
Advanced Numerical Linear Algebra	Design of Phase Locked Loops
Approximation of Dynamical Systems (MOR)	Analog Circuit Design
Random Processes and Applications	Semiconductor Manufacturing

PROFESSIONAL ACTIVITIES

- Student member, IEEE 2004-2009
- Reviewer, International Conference on VLSI Design, 2007
- Reviewer, Design Automation Conference (DAC), 2005, 2006
- Reviewer, International Symposium on Circuits and Systems (ISCAS), 2006
- Reviewer, Journal of Circuits, Systems, and Computers (JCSC), 2005, 2006

REFERENCES

Available upon request.